Eavesdropping On Mars – *V 1* – Part 3. (Words = 3443)

Ian Scott ZL4NJ

SciHigh@xtra.co.nz

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Circuit Topologies For X-Band Receiver System Stages

In part 2 of "Eavesdropping on Mars" I described a system design methodology navigated using key design drivers, followed with correspondingly appropriate specifications and presented two system design contenders. This methodology ensures a smooth design flow based on objective considerations. Can the application of such design philosophies be shown to provide profitable guidance using this X-band receiver as an example?

In this article, each RF frequency conversion system block is assigned a schematic. This allows sub-circuit isolation for critically assessment (attempting to complete an overall schematic in one step is likely to result in design oversights). Further, designers can focus on interfacing issues between sub-circuits. To illustrate, adding "dummy" coupling capacitors allows stages to be designed separately and tested separately after construction. These capacitors can remain in the final design due to their

insignificant cost. This assists fault finding if accidental solder shorts occur. Dummy capacitors can be also be used for optimising impedance match accuracy later on, if desired.

Circuit simulation also benefits. Determining where appropriate input and output nodes reside in a maze of circuitry can be unclear. By partitioning the design at the onset, stages can be optimised in isolation. Further, attempting to simulate an entire receiver is unlikely to be useful as overall performance deficiencies can't be attributed to individual stage faults.

Each sub-circuit will now be described, starting at RF input and ending at IF output. The stages are LNA1, BPF1, LNA2, BPF2, SHM, IF-Amp, LPF. The final schematic will then be presented at the end of this article. In part 4 I will approach the frequency synthesis system similarly.

SiGe Bipolar LNA1 Using BFP840

Infineon's BFP840FESD Silicon Germanium bipolar transistor may represent the highest performing HBT (hetero-junction bipolar transistor) on the market today. This inexpensive part is supplied in a 1.2 mm by 1.4 mm 4-lead TSFP-4-1 package and boasts a transition frequency of F_T = 85 GHz. It claims an unmatched power gain of $|S_{21}|^2$ = 15 dB at f = 8.5 GHz with an associated noise figure of $NF_{50} \sim$ 1dB. This improves

slightly when the device is matched for optimum noise figure (e.g. NF_{opt} ~ 0.95 dB). The device is well suited for amplification on lossy FR4 substrates ashigh Q matching structures required by HEMT (FET) devices are avoided. It should be noted that the published noise figures of many devices are not those measured on breadboards. Instead, the manufacturer “de-embeds” their measurement by subtracting the estimated PCB and matching losses. For example, a device noise figure published as NF = 0.5 dB could have been measured at 1 dB or higher in circuit!

Further, high Q matching structures may require manual adjustment and this is contradicts previously identified design drivers. Optimum adjustment implies access to expensive test equipment, also contrary to previous drivers. At $1.00 each (Digikey), the BFP840 provides cost effective, high performance amplification and avoids manual adjustment.

Although its maximum device voltage is V_{ce0} ~ 2V the BFP840 is internally protected against input power levels as high as +20 dBm. Its is also ESD hardened to survive 1.5 kV HBM. However, static discharge protection measures should still be observed when handling the device.

A suitable circuit topology is shown in Illustration 1. Simple resistor bias is adequate as the device NF is tolerant of bias variation.

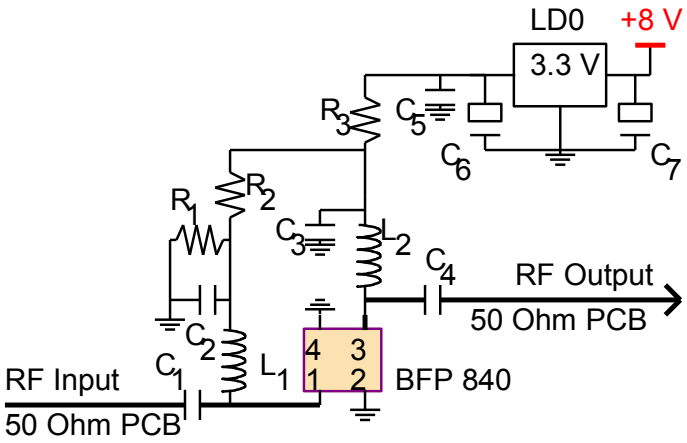

Illustration 1: Low Noise Amplifier 1 Using BFP840

The DC conditions will be defined at V_{ce} = 1.5 V, I_c = 10 mA. SiGe devices don't tolerate high collector voltages but V_{ce} = 1.5 V is comfortable. Collector current is non critical, I_c = 10 mA will result in reasonable power gain $|S_{21}|^2$ ~ 15 dB at f_c = 8.45 GHz, with associated noise figure NF_{50} ~ 1.1 dB.

Interestingly, it might be thought that a combination of Silicon with Germanium would result in a forward bias voltage somewhere between the two. Not true! It appears that the two "traditional" forward voltage "values" add. In practice, the V_{BE} of a SiGe bipolar will be closer to V_{BE} ~ 0.7 + 0.1 V = 0.8 V. From this, it is sensible to set $R_1 = R_2$ = 10 kΩ, leaving R_3 to drop 3.3 – 1.6 = 1.7 V. Setting I_c = 10 mA implies R_3 = 170 Ω. A practical value is R_3 = 180 Ω.

Capacitors C_1 and C_4 act as DC blocks that could also be used for impedance matching. Suitable values are $C_1 = C_4 = 4.7$ pF for $f_c = 8.45$ GHz. Capacitors C_2 and C_3 provide base and collector RF decoupling and capacitor C_5 provides additional supply decoupling at $f_c = 8.45$ GHz. Convenient values are $C_2 = C_3 = C_5 = 100$nF. Inductors L_1 and L_2 provide a DC path with medium RF impedance at $f_c = 8.5$ GHz. Suitable values are $L_1 = L_2 = 10$nH. A caution at this stage is timely; instability can easily result for any amplifier with similar, potentially resonant circuits at input and output! Although oscillations may be far removed from the intended operating frequency, nothing beneficial will occur. For example, erratic noise figure performance is likely. Also, oscillation frequencies may fall on a spurious response, causing receiver desensitising. In extreme cases, excessive voltage excursions could degrade the device or destroy it! It is advisable to include a protective resistance in series with each inductor. Using a 10 Ω resistor is sensible

A simple linear voltage regulator is used to reduce the +8V input supply to a safer level at 3.3V. Capacitors C_6 and C_7 are included to ensure LDO stability. This component is non critical and the designer can select their personal favourite.

C_1 and L_1 can also be used for "video decoupling" enhancing linearity, although this enhancement is not identified in the previous design drivers. However the method involves no cost and is applicable to other design projects. It has been shown by various authors that linearity is improved when the base is presented with a low impedance at difference frequencies associated with 2-tone third order intermodulation tests. In both theory and practice, intermodulation products can be reduced by as much as 20 dB! In this circuit, selecting a high value for C_2 and a low value for L_1 accomplishes this enhancement.

Comparison With Other Candidate LNA Devices

Device manufacturers tend to focus on particular technologies of choice. For example, Infineon is closely aligned with SiGe HBT devices. This is understandable following their introduction of the world's first mass producible SiGe device (BFP620) at a time when CMOS reigned. In contrast, CEL specialises is HFET device technology, with an example NE3512S02 boasting NF_{opt} = 0.35 dB, Ga = 13.5 dB at f = 12 GHz. However this device performance may have been de-embedded from actual measurement and actual circuit performance will therefore be worse. A further detraction is the need for a negative gate bias supply and potential measures to delay the application of drain voltage supply before this protective bias is available. Other suppliers such as Skyworks

straddle the game to some extent with cascadable devices based on InGaP such as the SKY65013-92LF. This device offers “broadband” gain to 12 GHz combined with exceptional linearity. Skyworks also has FET IC devices available such as the SKY3009-11 RF→IQ demodulator IC. Recently, Avago has announced a line of ultra miniature PHEMT devices operating up to 11 GHz with 20 dB gain and noise figures as low as 1.5 dB. Attractive as these may seem, the package dimensions are 1.0 mm x 0.5 mm. It is unlikely that these devices could be hand soldered without the aid of a microscope!

All device technologies have advantages and disadvantages. Based on previously identified drivers, SiGe best suits the design described here. Infineon's BFP840 is inexpensive, operates from a single positive supply, avoids impedance matching requirements and is suitable for placement on standard FR4 substrates. Although some slight improvement in noise figure is available from other technologies, these impose overheads and may necessitate relatively expensive low loss substrates.

Image Rejection Band Pass Filter 1 using BFCN-8450

The BFCN-8450 from Minicircuits provides a convenient solution for image rejection. This component comes in a small 3.2 by 1.6 mm SMD package. Its passband is 8.4 to 8.5 GHz with 1.6 dB loss (compatible with

the receiver specification). Stop-band attenuation exceeds 20 dB from from DC to 7.5 GHz and 10 GHz to 15 GHz. At $US 3.95 each for quantities of 20 units, this component represents an attractive alternative to conventional helical filters and avoids manual adjustment. The component is shown in illustration 2.

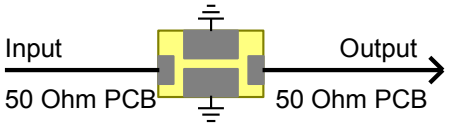

Illustration 2: Image Rejection Filter 1 using BFCN-8450

MMIC LNA using LEE-39+ or GALI-2

Minicircuits provides excellent MMIC gain blocks that operate well at 8.5 GHz. The LEE-39+ comes in a 3 by 3 mm SMD package and offers 13.5 dB power gain at f = 8.5 GHz with noise figure NF = 2.4 dB (relatively low compared to standard MMIC amplifiers). The GALI-2+ uses a popular SOT-89 package, offering 13 dB gain with NF = 4.6 dB. At $US1.19 and $US0.99 respectively (for qty=20), both offer economic broad band amplifier solutions.

The second LNA using the LEE-39 MMIC is shown in illustration 3. The circuit also applies to the GALI-2+ MMIC. Both operate from a +8 V supply using simple resistor bias.

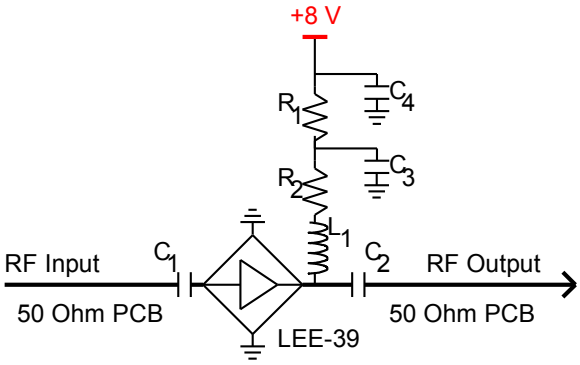

Illustration 3: Second RF LNA using LEE-39 MMIC

Resistors R_1 and R_2 should total 133 Ohms (e.g. 33 Ohms, 100 Ohms) for the LEE-39 and 113 Ohms for the GALI-2 (e.g. 56 Ohms, 56 Ohms). The MMIC devices are tolerant of bias variation the resistor values need not be exact. In principle, video coupling could be applied to MMIC devices to enhance linearity. However this objective is not indicated here.

Remaining components are non critical. For coupling capacitors and bias inductors, it is convenient to apply a "10:1 reactance" approach. Consequently $C_1 = C_2 = 4.7$ pF, $L_1 = 10$ nH for $f = 8.45$ GHz. Supply decoupling capacitors can adopt popular values such as $C_3 = C_4 = 100$ nF.

Image Rejection Band Pass Filter 2 using BFCN-8450

The second image rejection band pass filter is shown in illustration 4.

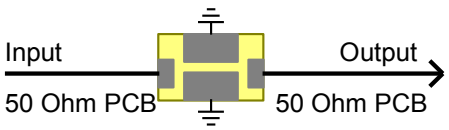

Illustration 4: Image Rejection Filter 2 using BFCN-8450

Sub Harmonic Mixer using BAT15-03W Anti-parallel Diodes

Sub harmonic mixing provides a convenient method that reduces high frequency VCO and frequency divider IC requirements. Unlike conventional double balanced mixers (DBM), the local oscillator (LO) frequency is injected at ½ the conventional LO frequency (although other integer sub-ratios can be used).

Sub harmonic mixers (SHM) can adopt either series or parallel topologies. The series implementation best suits PCB microstrip implementations whilst the parallel form suits lower frequency operation with lumped element L-C combinations. The series microstrip form is shown in illustration 5.

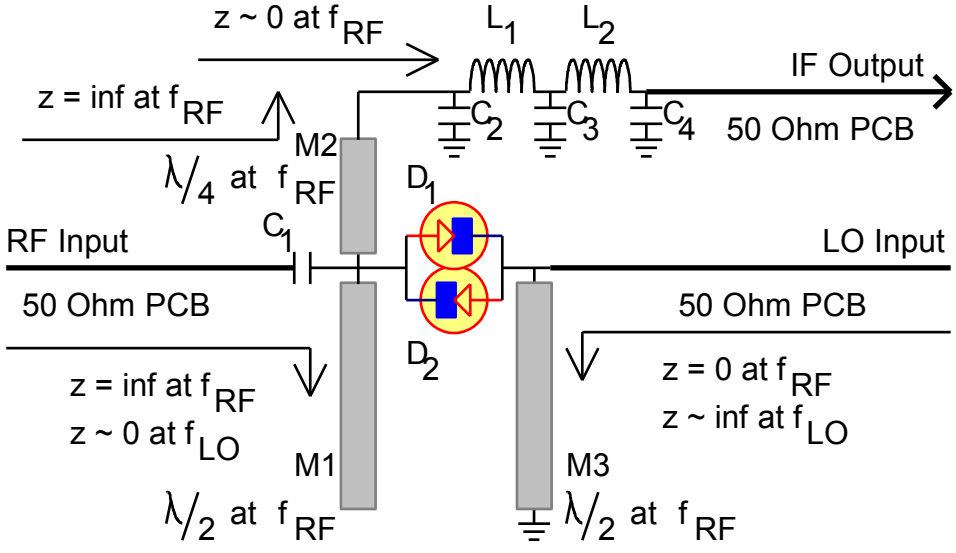

Illustration 5 - Sub Harmonic Mixer (SHM) using Series Anti-parallel Diodes

This microstrip approach uses open and short circuit terminations to isolate RF, LO and IF signals. M1 is a half wavelength long at the RF

input frequency ($\lambda/2$ at f_{RF}) presenting an open circuit to this signal, allowing full RF energy transfer. Microstrip M2 is a quarter wavelength long at f_{RF}. Since M2 is terminated by C2, effectively providing a short circuit at f_{RF}, it presents a high non-impending impedance to the RF signal. The IF signal is generated at this node. Microstrip M2 provides a transfer path for this IF signal to the IF LPF beginning with C2.

Microstrip M3 is one half wavelength long at f_{RF}. Since it is terminated with a short to ground, it presents a low impedance to the RF signal. Consequently, all RF energy supplied flows from RF input, through D1 and D2 that are effectively terminated to ground.

The LO frequency is approximately ½ f_{RF} and therefore M3 will appear as a near quarter wavelength ($\sim\lambda/4$ at f_{LO}), terminated by a short to ground. Consequently, transfer of LO energy to D1 and D2 will be relatively unimpeded by M3. After passage, this energy encounters M1, approximately a quarter wavelength long at the LO frequency. Since M1 is not terminated, it will appear as a near short circuit to this LO energy. Consequently, almost all LO energy is transferred to the anti-parallel diodes D1 and D2.

The interplay between M1, M2 and M3 therefore provides effective diplexer functionality for RF, LO and IF signals. Unlike standard DBM devices, the operation is narrow band. The microstrip dimensions are selected to favour efficient RF energy transfer so as to minimise SHM conversion loss. Efficient transfer of LO energy is treated as a secondary requirement since generating additional LO energy is not problematic.

The role of C1 may be unclear. Diodes D1 and D2 will have parasitic lead inductance, potentially degrading mixer performance. Capacitor C1 is selected to resonate with this inductance at f_{RF}. Since M1 and M2 present high impedances to the flow of RF energy, they are transparent. For example, the BAT15-04W SOT323 package has 1.4 nH inductance per diode and therefore 0.7 nH for the anti-parallel pair. At f_c = 8.45 GHz, this implies that C1 ~ 0.51 pF.

The IF signal is extracted through M2, being is a quarter wavelength long at f_{RF} ($\lambda/4$ at f_{RF}). It requires a near short circuit end-termination, provided by capacitor C2, heralding the input of the subsequent low pass IF filter comprised of C2, L1, C3, L2 and C4. SHM operation does not need this LPF but LO leakage could conceivably cause problems in a IF receiver if it falls on one of its spurious responses.

Since this LPF is an optional, non critical low pass filter, the simplest design approach is to implement it as two cascaded π-sections. This implies that all reactance values can be set to $X_k = 50\ \Omega$ (the centre capacitor will use $X_3 = 25\ \Omega$). Selecting the centre IF frequency $f_c = 1.25$ GHz, we obtain $C_2 = C_4 = 2.55$ pF, $C_3 = 5.1$ pF, $L_1 = L_2 = 6.37$ nH. These values may be adjusted to compensate for parasitic terms.

We now need to determine PCB microstrip dimensions. We can determine the half wavelength microstrip length $L_{\lambda/2}$ (in meters) using equation (1) with f_c representing frequency in Hz and ε_r defining the relative permittivity of the PCB substrate (typically 4.8 for FR4).

$$L_{(\lambda/2)} = \frac{3 \times 10^8}{2 \times f_c \times \sqrt{\varepsilon_r}} \quad ...(1)$$

At the centre RF frequency $f_c \equiv 8.45$ GHz, the half wavelength PCB tracks for M1 and M3 are $L_{\lambda/2} = 8.10$ mm. The quarter wave track for M2 becomes $L_{\lambda/4} = 4.05$ mm. However how wide should the microstrip elements be?

There are several equations that predict PCB microstrip characteristic impedance Z0 from track width W, substrate height H, copper thickness

T and relative permittivity ε_r. Of these, a relatively simple, but adequately accurate version is shown in equation (2), with all dimensions in meters

$$Z0=\frac{87}{\sqrt{\varepsilon_r}+1.414}\times\log_e\left(\frac{5.99\times H}{0.9\times W+T}\right) \quad ...(2)$$

Setting $\varepsilon_r = 4.8$, H=0.6 mm, T=0.05 mm and W = 0.9 mm results in Z0=49.9 Ω, suitable for M1 and M3. The microstrip M2 can adopt a higher characteristic impedance since it operates as a choke, and setting W=0.5 mm predicts Z0=68.8 Ω. This width is convenient as it equals the pin spacing in many modern SMD packages such as 16-VFQFN, as used with the SY89231u frequency divider IC (division ratios = 3 or 5).

The SHM can also be implemented in its parallel diode form using lumped element components. An example is shown in illustration 6.

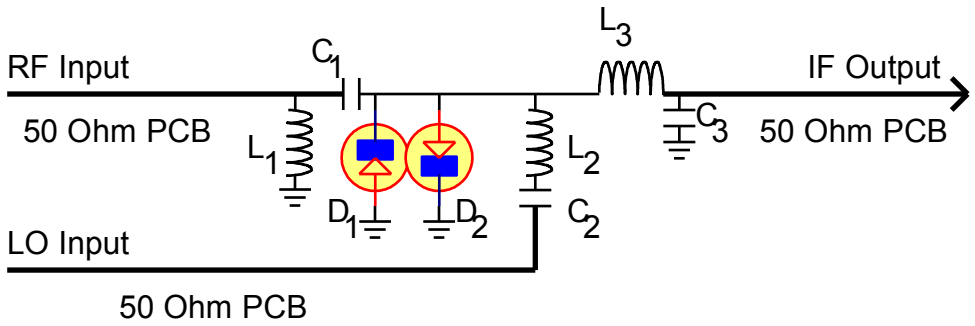

Illustration 6: Sub Harmonic Mixer (SHM) using Parallel Anti-parallel Diodes

This lumped element L-C based form uses high pass, band pass and low pass filters to isolate RF, LO and IF signals. The RF input signal is transferred to the anti-parallel diodes through a high pass filter comprised of L_1 and C_1. The lower IF frequency uses low pass filter L_3 and C_3 to transfer energy to the IF output port. Local oscillator injection is coupled to the diodes through a band pass filter consisting of L_2 and C_2.

In this configuration, termination impedances are not “exactly” defined. For example, the IF LPF only presents a moderate impedance to incoming RF energy resulting in some RF energy loss. Equally the RF HPF only presents a moderate impedance to LO energy, resulting in some LO energy loss. Finally, the extracted IF output energy competes with the parallel load impedance presented by the input HPF. All three mechanisms conspire to increase conversion loss.

Adding frequency notches may help to some extent. For example, adding a capacitor in series with L_1 that resonates at the IF frequency will potentially reflect energy back to the anti-parallel diode pair via C_1. Similarly, adding a capacitor across L_3 that resonates at the RF frequency will result in an infinite impedance, rendering RF energy loss negligible.

Although the series form may seem superior in all respects, when implemented at lower frequencies the PCB transmission lines can become unrealistically long. This is a moot point as the need for a SHM at lower frequencies is unwarranted and standard DBM devices represent a superior choice!

Comparing SHM and DBM Configurations

Sub harmonic mixers (SHM) are narrow band systems compared to their much wider double balanced mixer (DBM) cousins. They are relatively easy to implement and avoid the need for RF transformers. Conversion loss is higher than the DBM (10 ~ 15 dB). Linearity is similar but since the X-band receiver is intended for a weak signal environment, this attribute is otherwise unimportant.

The architecture described could employ a conventional DBM device but a frequency doubler would be needed to generate a suitable LO signal, increasing complexity. DBM devices are plentiful and can be dropped in the circuit with little design consequence. However the design of stable, efficient frequency doublers present an additional design challenge. Is designing a SHM more difficult than designing frequency doubler? Both approaches present similar levels of design risk or intrique.

Spurious Response Predictions

The SHM exhibits greater conversion loss compared to standard mixers and requires additional RF gain. Linearity is similar (although not required for weak signal operation). The SHM has a greater number of potential spurious responses but only linear spurious responses are relevant here. However it may be interesting to consider its equivalent "½ IF" response exhibited by all mixers. To illustrate consider f_{RF} = 8.4 GHz, f_{LO} = 3.6 GHz → f_{IF} = 1.2 GHz. Now apply f_{RF} = 7.8 GHz → f_{IF} = 0.6 GHz. The second harmonic of f_{IF} = 1.2 GHz corresponds to a ½ IF spurious response. In formal terms, $f_{IF}=2\times f_{RF}-4\times f_{LO}$ i.e. this can be referred to as a (2,4) spurious. Since it is a non linear response, its magnitude will vanish in weak signal environments and is unimportant.

Post Mixer IF Amplifier using LEE-39+

The post mixer IF amplifier can replicate the second RF LNA topology displayed in illustration 3. This sub-circuit is shown in illustration 7.

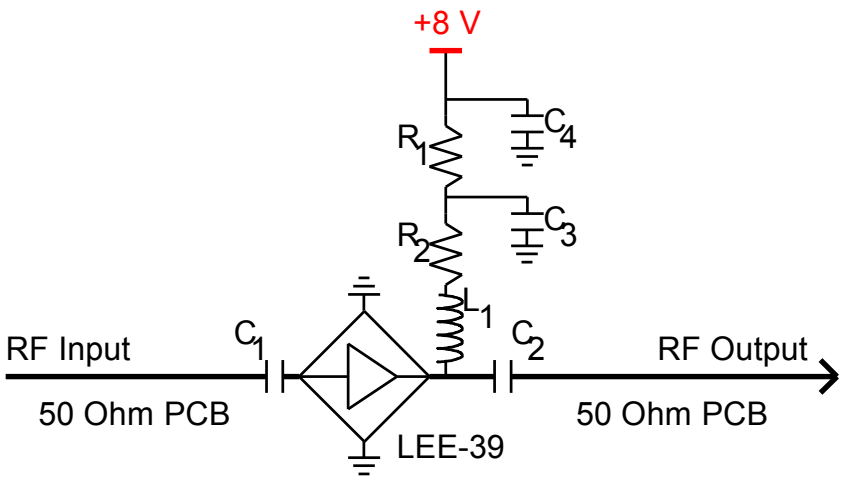

Illustration 7 - Post Mixer IF Amplifier using LEE-39 MMIC

The post mixer IF amplifier replicates LNA2. Capacitors C_1, C_2 and inductor L_1 are increased for reduced frequency operation at f_c = 1.25 GHz. Suitable values are $C_1 = C_2$ = 47 pF, L_1 = 100 nH. Decoupling capacitors are non critical so that $C_3 = C_4$ = 100 nF should be suitable. The expected IF power gain will be $|S_{21}|$ ~21 dB.

Final Output L-C Based Low Pass Filter

This filter provides addition protection for the IF receiver's spurious responses. A simple “Tee” configuration is shown in illustration 8.

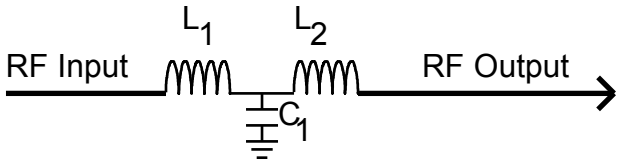

Illustration 8: Final Precautionary IF LPF

The simplest approach is to define each component value to have a reactance of X_k = 50 Ω at the centre IF frequency (f_c = 1.25 GHz). Consequently C_1 = 2.55 pF and $L_1 = L_2$ = 6.37 nH.

Complete RF Schematic

A complete schematic, drawn with ExpressPCB is shown in illustration 9.

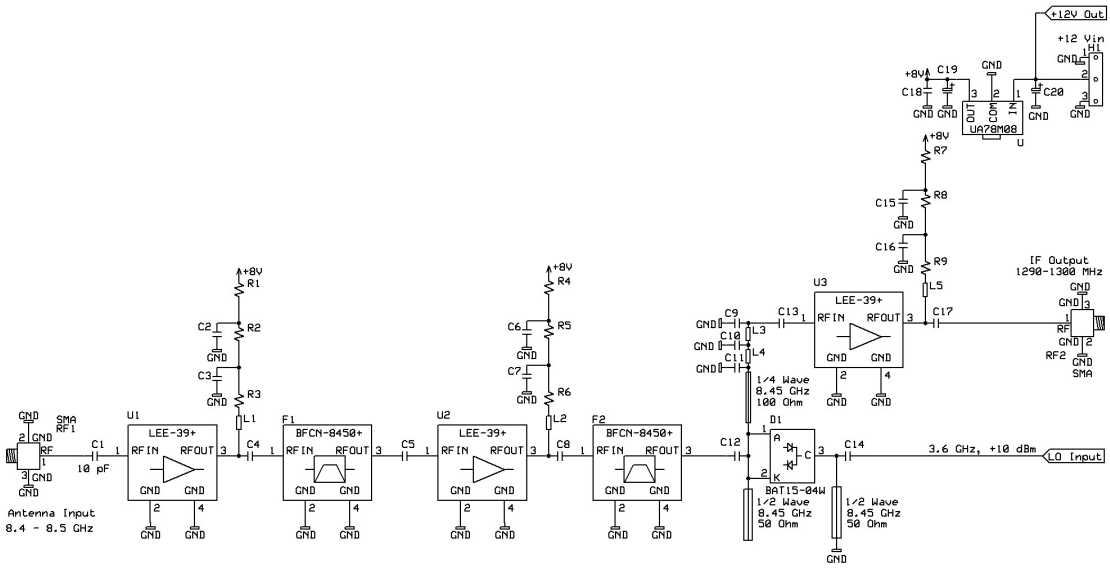

Illustration 9: Complete RF to IF Converter Schematic

The schematic shows two cascadable MMIC amplifiers with two fixed image reject filters. The SHM is implemented with a dual Schottky diode and three microstrip terminations. Additional IF gain is included.

Summary

Typical circuit topologies have been shown for each RF to IF system block described in part 2. These have then been combined into a single RF down-converter schematic. The frequency synthesis sub system will be described in part 4 and use a similar approach. This article will also include the RF down converter schematic. Both schematics will contain final component values. Looking further ahead, I intend to describe PCB layout details in part 5.